ACE MEETING, June 29, 2004

- Tevatron Status
  - Tevatron had record delivered luminosity last week even though one store ended early due to human error and another due to an earthquake!
  - Tevatron studies will take place this morning followed by a "mixed-mode" shot with some pbars from recycler and some from accumulator.
  - Rest of week should be "stack and store" with occasional pbar studies in the background.

- Miscellaneous Ace Items
  - Please remember that the two ACES are often the most knowledgeable people in the Control Room. Question authority when necessary. (SciCos are not suppose to go offsite to get dinner for example....)

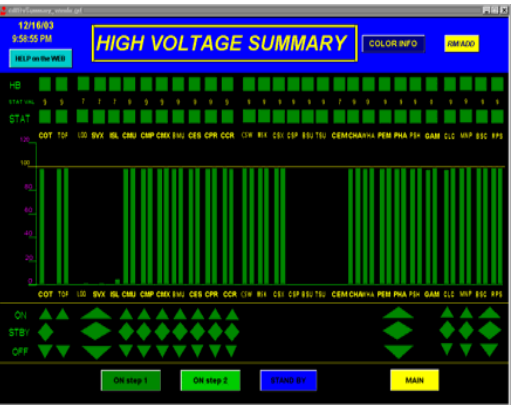
- Silicon Issues - Rainer Wallny

What You should know about the Silicon

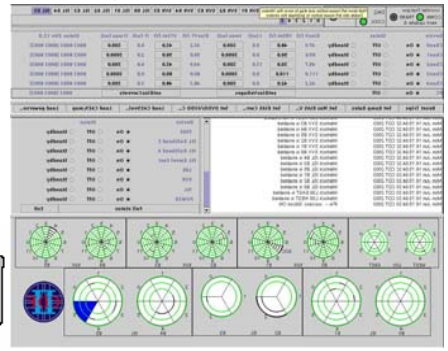
Ace Training recap I:

IFIX and Power supplies

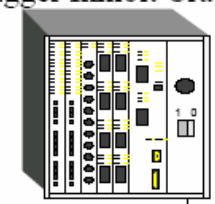
The Power Supply System



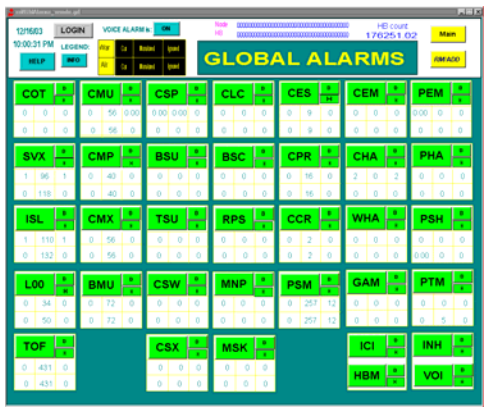
Gui-IFIX Comm

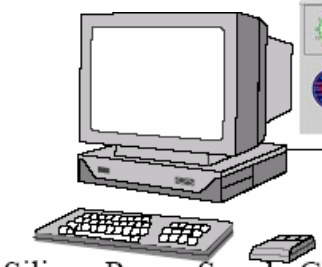


Trigger Inhibit Crate



Inhibit Patch Panel





Silicon Power Supply GUI

2nd Floor East Rack

Kill Switches

PS Interlocks

Crate Reset

SVXINTER (VME)

CAENet V288 Controller

CAEN SY 527 Crate

LV,Bias, Remote Sense

90 Pin Junction Card

FIB Timing

Delay Box

FIB Crate

Silicon

Inside CDF

Power Supply Mantra

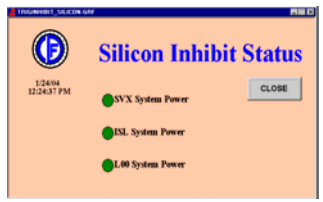
- There are 16 CAEN power supplies in the collision hall. They don't quite always correspond to the subsystem they belong to because … never mind.
- The provide the following voltages to the silicon ladders:
  - AVDD (per ladder)
  - DVDD (per ladder)
  - 2V/5V DOIM (per 'wedge')
  - Bias0/1 (per 'ladder')

STANDBY:ON

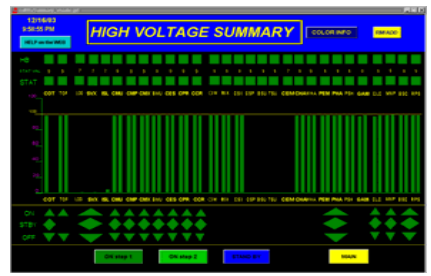
STANDBY:OFF

ON: both STANDBY+BIAS=ON

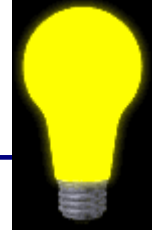
- A ladder can draw too much current on any of these voltages and then trip.
- **Tripped** != **OFF**. Tripped is special a 'state of mind', ie. a condition of the channel in the CAENs. This condition is picked up by the trigger inhibit system which is a piece of hardware and FAST-> hardware trigger inhibit.
- IFIX should know everything about the state of the system, including its trip state. So IFIX is another source of 'knowledge' about the state of a ladder.
- In particular, the silicon IFIX PC performs a sanity check of the bias voltages read back from the CAEN system. If the bias voltage is <90% of the nominal, it issues a SLOW software trigger inhibit.



- Incidently, the bars you see in the global alarm page, are the smallest and highest percentages of these readbacks – if one ladder is **OFF** or **TRIPPED**, one bar will be gone.
- It is a LEGAL STATE to have a ladder OFF but not TRIPPED – IFIX will be silent but the software trigger inhibit will fire.
- How you got there into this state is another matter …..

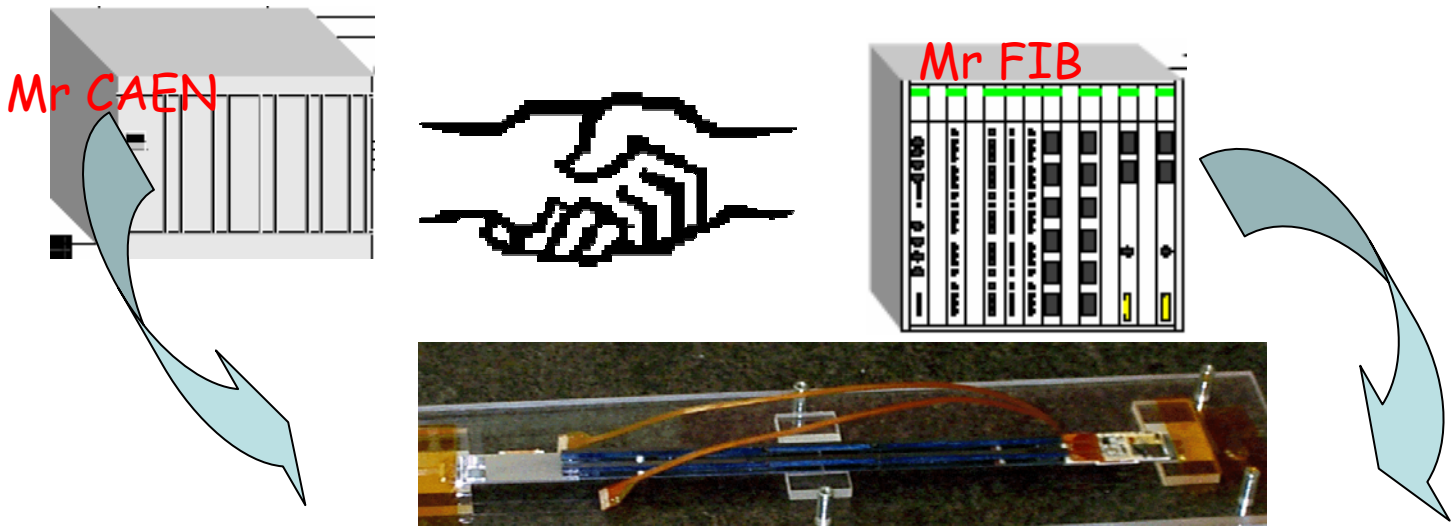


The Silicon is not a light bulb ….



i.e. a ladder is not just simply switched ON like the latter:

- chips need to be initialized immediately on turn on
  ⇒ Readout (FIB) and Power supply need to conspire
- "Ready to turn ON ? " - "Ready!"
- "Turning on …" "Ah, I see some current! Initialize!"



Problem:

- Mr FIB in ACTIVE listens only to Run Control!
  => normally get ERROR: Power Supply ISL/SVX/L00 Bx Wy Handshake -No response from the FIB
- Need to put DAQ in HALT to free up Mr FIB's ears to do the handshake

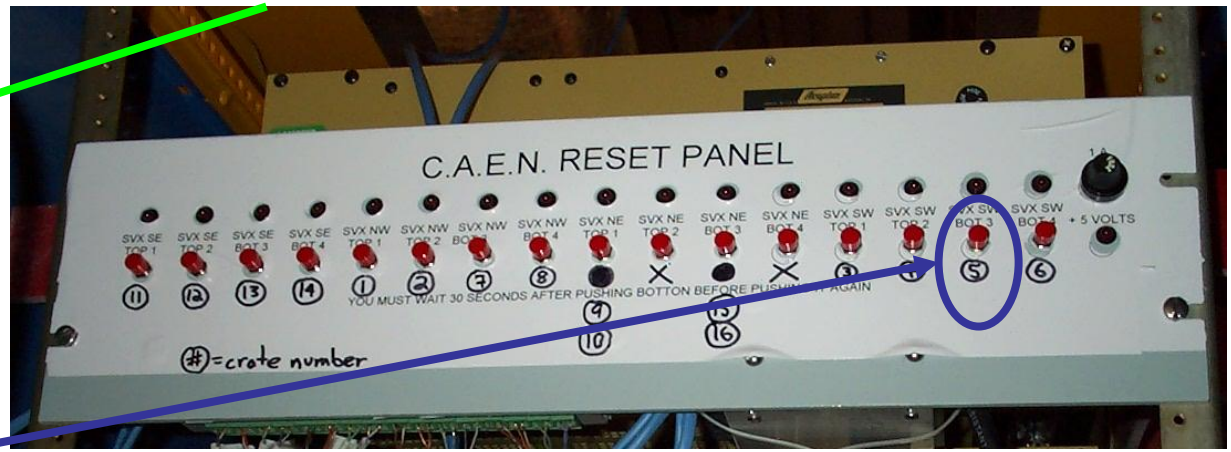
CAEN crate communication failures (aka crate 'Hockerization')

He Who Used to Hocker the crate …

1. IFIX alarm/trigger inhibit

DEVICE	DESCRIPTION	LOW ALARM	LOW WARNING	CURRENT VALUE	HIGH WARNING	HIGH ALARM	IGNORED?
SVX POWER SUPPLIES (see GUI)							
PS-TRIP	This field filled at alarm time			OK			NO
PS-ALARM	Crate 5 communication failure			ALARM			NO

2. Note crate number
3. If running w/ silicon, bring run to HALT state
4. Go to rack 1RR34G (easternmost row of racks in 1st floor counting room)
5. Plug in reset power supply (labeled with a big tag)



6. Press crate's reset button for 1 sec
7. Wedges in the crate are now OFF, return to ON or STBY with buttons on IFIX HV page
8. After trigger inhibit clears, RECOVER and RUN
9. Unplug the reset power supply
10. Make note in e-log, page silicon if there are problems or if in doubt.

Soon to come:
Automatic Hockerization!

Power Problem Recovery Summary

Software and Hardware trigger inhibits can stop the run – (if everything goes right and the tools themselves don't misbehave). You are not expected to be able to fix all of these but you should be able to transfer the relevant information to the expert on the phone.

1) Ladder or PS trip:
- IFIX Global alarm on PS TRIP condition
- Red wedges/ladders in PSGUI
- Red squares in IMON
- Software and Hardware trigger inhibit
- At least on bar down in HV summary page

2) Crate communication error:
- IFIX Global alarm on crate communication error
- Software trigger inhibit and (maybe) hardware trigger inhibit as well
- wedges grey in PS GUI
- BLUE squares in IMON
- At least one bar down in HV summary page

3) "Spontaneous transition" (could be glitch in communication)
- ladder/PS turns OFF but NO IFIX Global alarm
- software trigger inhibit (indicates offending ladder)
- At least one bar down in HV Summary page

4) GUI- IFIX communication error
- NO trigger inhibit
- All 3 subsystems L00,SVX, ISL red in Global Alarms Page
- Purple heart beat indicators in the HV Summary page

What You should know about the Silicon

Ace Training recap II:

Oy veh, the Sili DAQ …

Say NO!

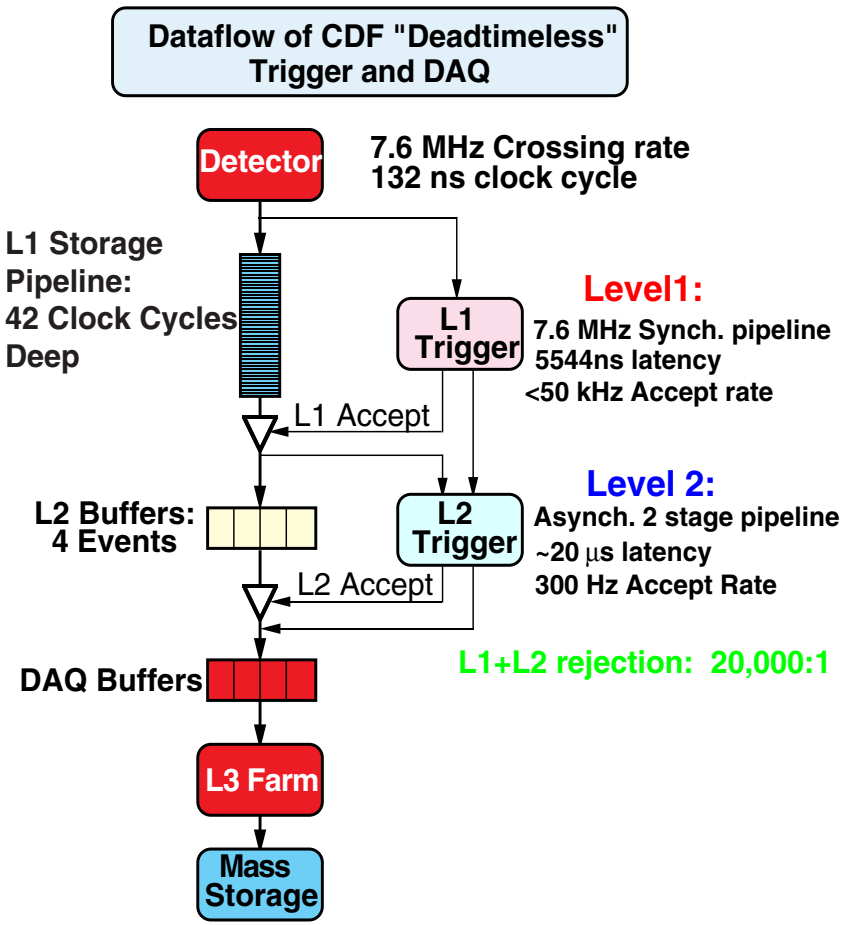
NO Silicon in NON standard trigger conditions w/o consent from pager carrier !

- regardless of what the expert says – they are experts of THEIR system, but (usually) NOT of the silicon
- They surely don't mind using a US$ 20 Mio device to debug theirs BUT do they really need the silicon to accomplish what they want ?
- Only situations where silicon can be included by default without pager carrier consent:
  - During 'normal' data taking with silicon biased, and TevMon GREEN signal
  - During quiet time for cosmics running (silicon biased), when it is made sure MCR does not inject beam into the machine without notifying us.

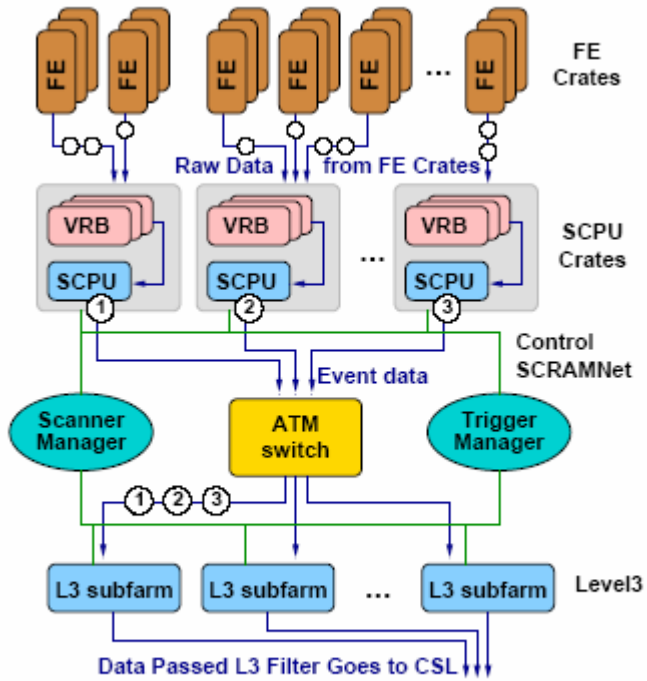
IF IN DOUBT: PAGE THE PAGER CARRIER OR SPL

- Usually the OpsManager was made aware of the request and has already consulted with Silicon people.

Review of Trigger/DAQ

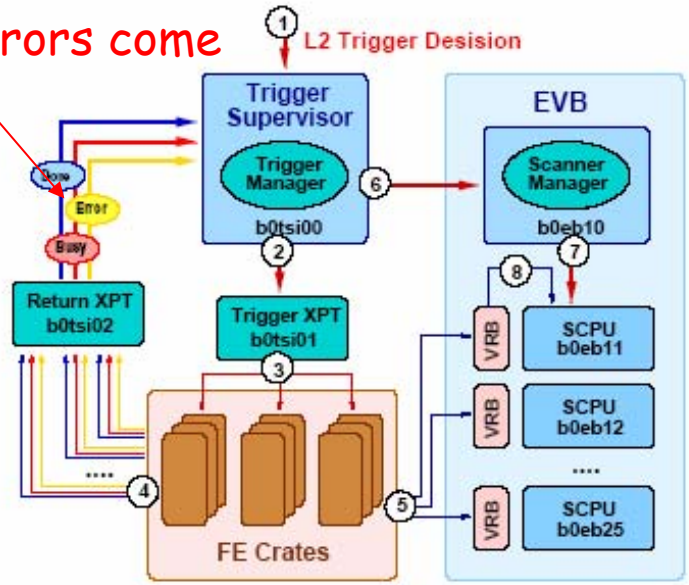


- Detector 'samples' data every 132 ns
- 'Samples' are stored in a pipeline buffer
- Data is sent to the Level1 trigger
- trigger decides within trigger latency of ~4μs
- If event is kept, data is stored again in L2 buffer still in front end awaiting L2 decision within ~20 μs (**not** for silicon)
- If L2 Accept, copy data into DAQ buffer and further up the chain.



DAQ Overview (from Ray Culbertson)

This is where our fatal errors come from



The L2 Trigger sends the trigger decision to the Trigger Supervisor (TS).

The L2 trigger decision is sent to the FE crates through the trigger cross point.

When the trigger decision is received in the FE crate, the VME Readout Controller (VRC) sends back a DONE signal to the TS via the return cross point indicating that it is ready to receive the next trigger decision.

We have an SRC

Not Si: Silicon reads out to VRBs on L1

Data from the FE cards (TDCs, ADMEMs...) is formatted and sent via the TRACER to the VME Readout Buffers VRBs.

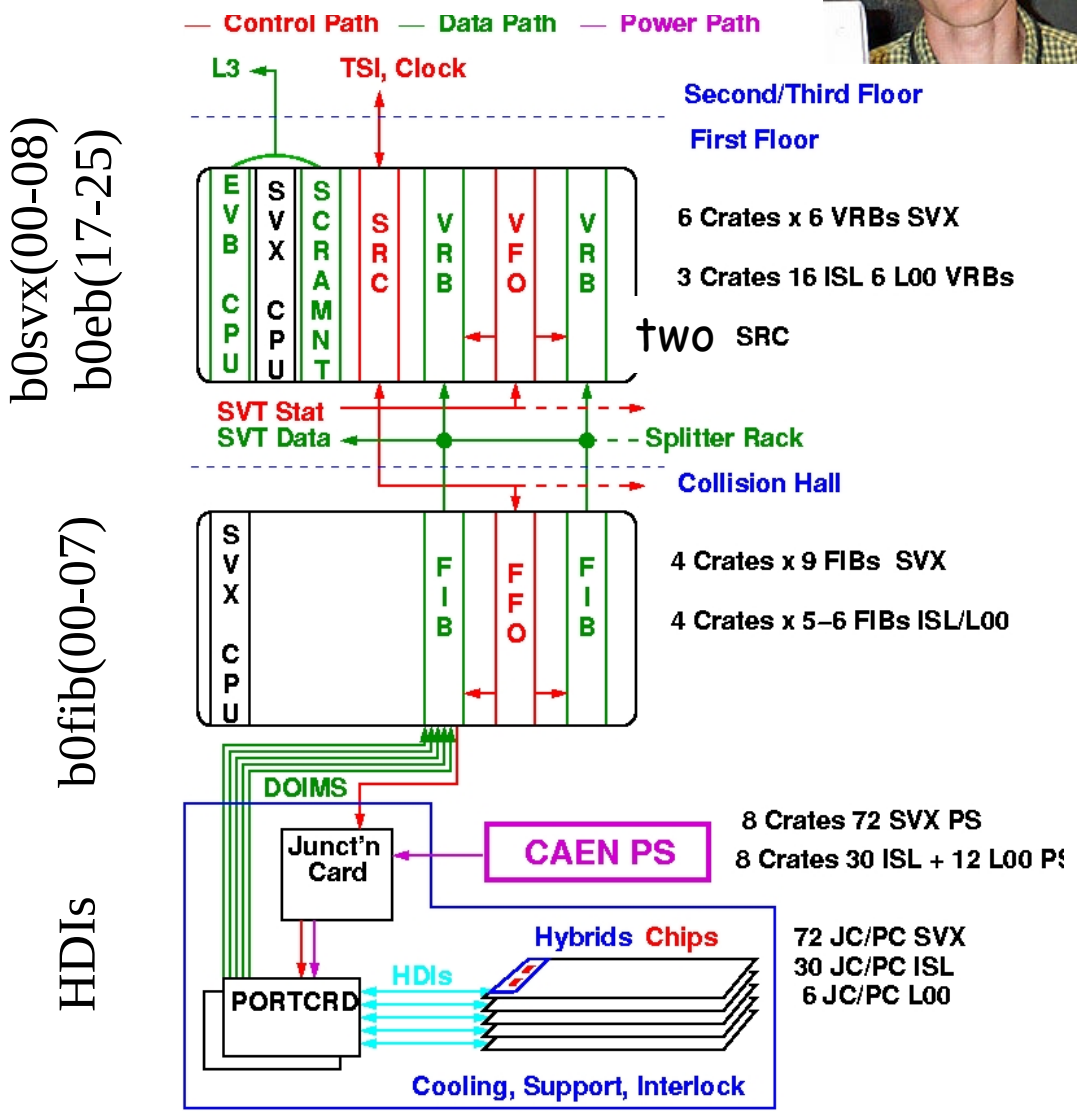
If there is not enough space to write out the event to the VRB a BUSY signal is sent back to the TS so that the TS does not issue another trigger which leads to busy deadtime.

→ If the busy is not deasserted in time we can get a Busy Timeout causing the run to halt.

This guy knows it all =>

Silicon from the DAQ Perspective

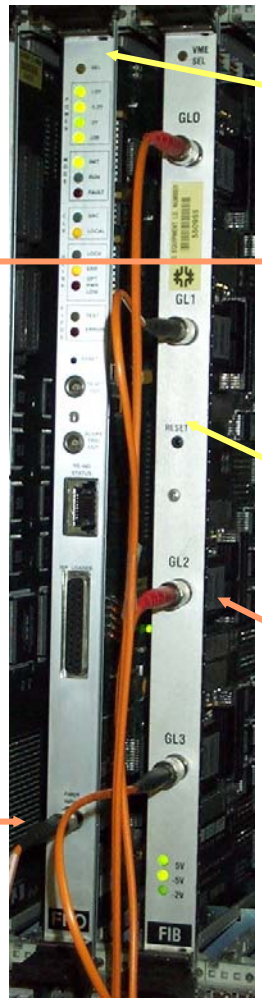
- **Silicon is different**
  - 17 crates, but TWO **SRCs** which talk to TSI
    - All **BUSY**, **DONE**, and **ERROR** timeouts come from them ***though problem may be elsewhere***
    - SRCs live in b0svx02 and b0svx06
  - Due to SVT, Si reads out to VRBs after L1A (not L2A)
    - VRBs are crucial
    - L1DONE signal to TS indicating data transferred to VRB
  - CPUs play role only in initialization and monitoring
  - b0svx** crates shared with EVB – you can't shepherd them and if you reboot them by other means, you have to clean the EVB!



Silicon Readout Controller (SRC) from Steve Nahn

- Controls what is going on when in the Silicon
  - Interfaces with the TSI for Trigger and Readout
  - Manages which buffers are in use, which are free, etc.
  - Responsible for "keeping the chip happy"
- Sends to FIBs and VRBs
  - Signals: Like L1A, PRD2 –Signals go "straight through"

Fiber Interface Board and friends (from Steve Nahn)



- Fib Crate contains
  - FFO: Conduit from SRC to *n* FIBs
    - Takes Glink optical signal converts it to 20 bits of backplane signal including Clock, Commands, Signals
    - Sends "Status" back to SRC
      - Used for Resonance detection
  - FIB: Mr Middle Man
    - Initializes Chips by VME
    - 10 x 8 bit DOIM input → 4 x 20 bit Glink output to SVT and VRB
    - Interprets SRC Commands via its Sequencer
    - Processes the Data read out

Bulk Memory – The VME Readout Board (From Steve Nahn)

- VRB crate contains
  - VFO: SRC ↔ VRB communication
  - VRB (running CDF SVX firmware)
    - Receives Data from FIB, store in (1 of max 12) buffers selected by SRC
    - Processes 16 bit wide data up to output (64 bits)
    - During readout → other VME access interferes

Silicon DAQ Runtime Errors

Run Time Errors: `Halt-Recover-Run` is first line of defense.

If anything persists, page Si pager. You might first see an error condition from a silicon crate – get more information on `HALT` when Si crates query all boards and find potential problems

i.e. `Silicon Timeout:BUSY- Slots: 10:fa00 12:fa20…`

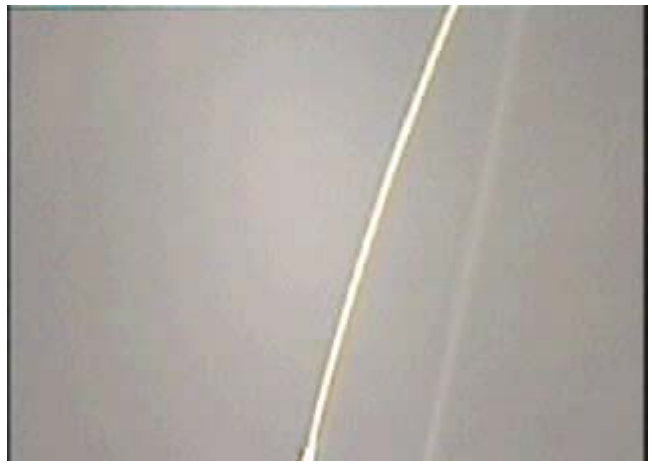
```
NOTE: on HALT will see also messages like
(MLE) b0svx04:Messenger:1:51:03 PM->Silicon Resonator:Sl 18 Ch 1 -> e481:
   Bytes: 00064
(MLE)b0svx00:Messenger:1:51:03 PM->Silicon Resonator:Sl 20 Ch 6 -> e0b1:
   Bytes: 00040
```

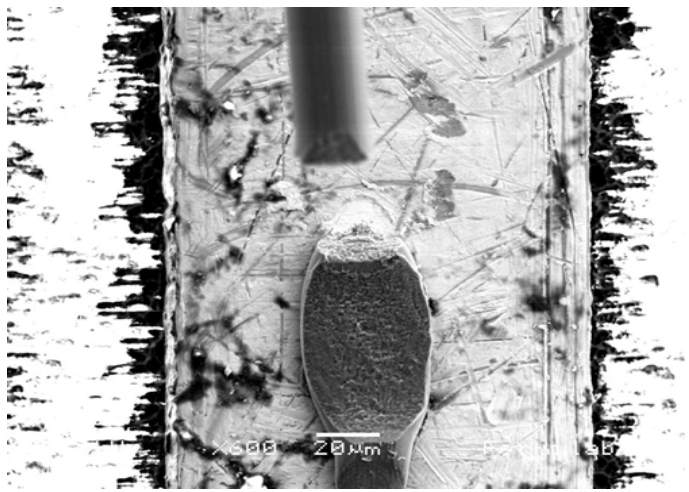
These are only meaningful if a resonance was detected, see below.

- `Done TO:` Data did not get sent to the VRB. Very rare, usually means a VRB is bad. Error handler
- `L1 Done TO`: TS has lost count of how many free buffers in Si Chips. Exceedingly rare.
- `Busy TO:` Means VRB has no more space for events. **Exceedingly common** , as **EVB** stops when any data corruption is detected **anywhere** (normally **NOT** in a Silicon crate) and the Silicon VRBs fill up first. Find data corruption and page responsible group.
- `Done TO from TRIGGER_SCALERS_00 Rate too high`: L1A rate too high to safely operate silicon. Usually trigger table is corrupt or there's a hot trigger. Page Trigger, look at TrigMon.

Resonant Lorentz Forces

- Resonance would accelerate fatigue
  - Fundamental frequency for 2 mm AlSi bond ~ 15 kHz
- We visually searched for resonance using test bonds in 1.4T field
  - Drive w/ sinusoidal AC
  - First resonance observed
    - ~19 kHz w/100 mA
    - Bonds move several times the wire diameter (~100 um)
  - Scan current (10mA-150mA)
    - Resonance present even at 10 mA.
- After exposure to resonance for minutes-hours, bonds break
  - Break occurs at foot of bond
  - Break is due to fatigue
- Tests confirmed with real modules driven by real DAQ





Silicon DAQ Runtime Errors (cont'd)

- SRC Fatal Error: Data taking has stopped due to a serious error condition – HRR should help.

  current SRC firmware ailment:

  SRC Fatal Error:Sl 5 L2A w/o L1A

  HRR out of it and make a note in the elog

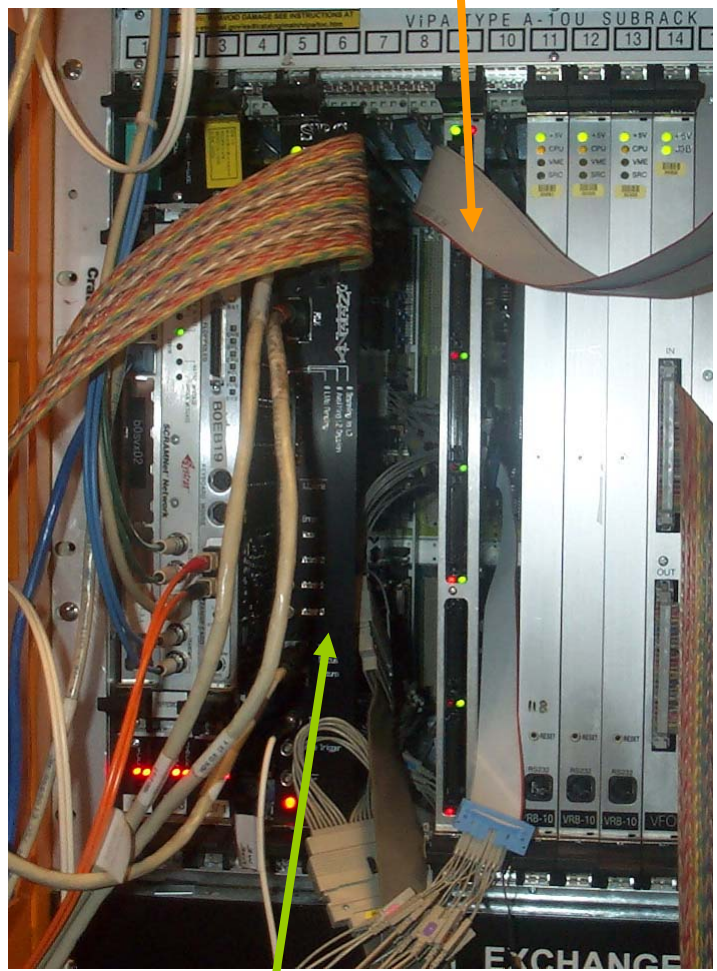
- SRC Fatal Error: SL 5 Resonance detected: A resonance condition was detected which is potentially harmful for the silicon. Note that only b0svx02 and b0turns RED first, then on HALT you will receive the error message.

  Additional information on HALT

  ```
  (MLE) b0svx04:Messenger:1:51:03 PM->Silicon
     Resonator:Sl 18 Ch 1 -> e481: Bytes: 00064
  (MLE)b0svx00:Messenger:1:51:03 PM->Silicon
     Resonator:Sl 20 Ch 6 -> e0b1: Bytes: 00040
  ```

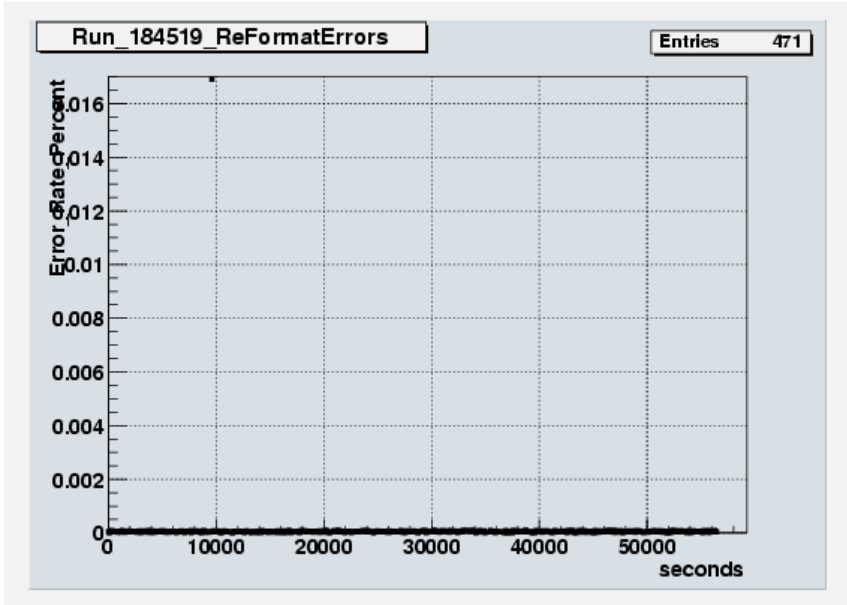
- RECOVER and RUN once, on 2nd time page silicon.

- Please discern these errors from the error logger information (example and example)



Reformatter errors

- We are the source of occasional (<=0.1%) reformatter errors
  - Problem is a low rate bit error in the ATM switch
  - Example run summary, error log, reformatter log
  - This is NOT a problem if it stays low rate.
- Try to discern new problems from this 'background' – make use of the various log files.



DAQ Summary

- (Si) DAQ is complicated business – but it pays in efficiency to understand
- Understand the meaning of the different states START, IDLE, READY, HALT and the respective transitions
  - In particular don't RESET if you don't have to
- Always consult the error logger/error log file
- Keep in mind unless you are in HALT you might only get half the story – ABORT is the same from this point of view.